WHAT IS CLAIMED IS:

1. A power transistor composed of a plurality of vertical PNP transistors formed on a P-type silicon substrate, wherein

a singularity or plurality of electrode portions of an N^+ type buried layer formed to isolate the P-type silicon substrate and the plurality of vertical PNP transistors from each other are provided in an active region of the power transistor.

2. The power transistor according to Claim 1, wherein

at least part of the electrode portion is provided under common emitter metal lines of the power transistor routed on the active region of the power transistor.

3. The power transistor according to Claim 1, wherein

the electrode portions are provided on the N^+ type buried layer and formed of an N^+ type electrode layer for making ohmic contact and an N^+ type diffusion layer.

4. The power transistor according to Claim 3, wherein

the N^+ type diffusion layer is formed simultaneously with an N^+ type base well layer as a base region of the plurality of vertical PNP transistors.

5. The power transistor according to Claim 3, wherein

the N^+ type diffusion layer is formed at a range of dopant level of 1×10^{16} to 1×10^{17} atoms/cm^3, which is heavier than that of an N-type epitaxial layer formed on the P-type silicon substrate.

6. The power transistor according to Claim 3, wherein

the N^+ type diffusion layer is formed so that dopants are diffused until they reach the N^+ type buried layer present on a bottom face of the power transistor.

7. The power transistor according to Claim 1, wherein

the singularity or plurality of electrode portions are placed so as to be uniformly spaced from their respectively adjacent electrode portions.

8. A semiconductor integrated circuit characterized by using the power transistor as defined in Claim 1.